FIFTH SEMESTER ENGINEERING DEGREE EXAMINATION

13.505 MICROPROCESSOR AND INTERFACING – MODEL QUESTION PAPER

TIME: 3 HRS   MAX MARKS: 100

PART A – *Answer all questions. Each question carries 4 marks.*

1. With suitable diagram, explain how the Address/Data bus (AD0-AD7) of 8085
   microprocessor is de-multiplexed.
2. Differentiate between memory mapped I/O and I/O mapped I/O.
3. What is an assembler directive? Which assembler directives are used to define a
   procedure and a macro? How is a macro different from a procedure?
4. What is the difference between Mode 0, Mode 1 and Mode 2 operations of 8255?
5. What are vectored interrupts? How is the address of the Interrupt Service routine
   calculated in vectored interrupts? Explain with an example.

                                                                          (5 X 4 = 20 marks)

PART B
Answer any *one* question from each module

MODULE I
6. a. Differentiate between partial and absolute address decoding. Give an example (10)
   b. Draw the architectural diagram of 8085 microprocessor and list out the following
      (i)   General Purpose Registers
      (ii) Special Purpose registers with their functions
      (iii) Flags in the flag register with required explanation   (10)
                                         OR
7. a. Explain the purpose of the following signals in 8085
      (i)   READY
      (ii) AD_0-AD_7
      (iii) HOLD
      (iv) IO/ M
      (v)   INTR   (10)
   b. Design a memory system for 8085 such that it should contain 2KB of EPROM and 2
      KB of RAM with starting address 0000H and 6000H   (10)

MODULE II
8. a, What is an addressing mode? With suitable example, explain any 4 addressing modes
   in 8085   (10)

b. Draw the timing diagram of a memory read bus cycle. Suppose the READY signal becomes low at the middle of second T state. Draw the timing diagram for the modified memory read bus cycle. (10)

OR

9. a. Explain the memory organization of 8086 microprocessor. Draw the timing diagram of a typical memory write machine cycle. (10)
   b. Draw and explain the architectural diagram of 8086 microprocessor (10)

MODULE III

10. a. Suppose [AX] = 85H and [BX] = 64H, [SP] = 2000H. What will be the value of AX, BX and SP after the following set of instructions are executed?
      (i) PUSH AX   b. POP BX (5)
    b. 10 numbers are stored from location 1000 onwards. Write an assembly language program to find the average of these. Draw the flowchart also. (10)
    c. What are maskable and non maskable interrupts. Give examples. How will you mask an interrupt in 8086? (5)

OR

11. a, 10 numbers are stored from location 1000 onwards. Write an assembly language program to count the number of odd numbers in these. Draw the flowchart also. (10)
    b. Suppose [AX] = ACH. What will be the value in AX in each of the following cases if the carry flag is set?
      (i) ROL AX,2   (ii) RCL AX,2 (5)
    c. Explain the operation of the DIV instruction. What is the difference between DIV and IDIV (5)

MODULE IV

12. a. With suitable diagram, explain how the Priority Interrupt controller 8259 can be interfaced with 8086 in cascade mode. (10)
    b. Draw and explain the block diagram of 8254 software programmable timer. Explain how the GATE input controls its operation in any two modes of operation. (10)

OR

13. a, What is DMA? Which hardware pins are used for DMA control? Draw and explain the architecture of 8237 DMA controller. (10)
    b. What is the advantage of using 8279 for keyboard/display interface? What are scan lines used for. Explain its following modes of operations
      (i) Encoded Scan Mode   (ii). Decoded scan mode (10)

(20x4 = 80 marks)