

FIFTH SEMESTER B.TECH DEGREE EXAMINATION

Branch: Electronics and Communication

13.506 ELECTIVE I: DIGITAL SYSTEMS DESIGN WITH VHDL (T)

Time: 3 Hours

Max. Marks: 100

Answer all questions

Part – A

1. Explain, with example, the meaning of concurrent and sequential coding in VHDL.
2. What is meant by implicit and explicit block statements in VHDL?
3. Write the data flow description for a 1 bit comparator. Output of the comparator should be equal to 1 when both inputs are equal, otherwise, 0.
4. Write a VHDL description for the generation of a clock signal.
5. Write notes on signal attributes.
6. Discuss constrained and unconstrained array types in VHDL.
7. Explain package and package body in VHDL.
8. Write a model for three input NAND gate with an inertial delay of 3ns.
9. List the differences between CPLD and FPGA.
10. Explain the use of technology libraries in VHDL synthesis. **(2×10 marks=20 marks)**

Part – B

MODULE I

- 11.(a) Explain with examples, the four classes of data objects . Clearly mention the difference between variable assignments and signal assignments. (10)
(b) Write short note on generate statement. Implement a 3:8 decoder in VHDL using generate statement. (10)

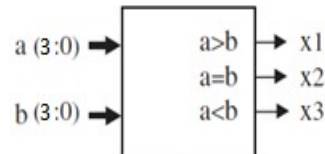
OR

- 12.(a) Discuss the three different styles of description in VHDL , taking the example of a 4:1 MUX . (10)

(b) Write short notes on
(i) Generics in VHDL.
(ii) Configurations (10)

MODULE II

- 13.(a) Explain operator overloading. Write a package that provides two overloaded functions for the plus operator. (10)
(b) What are the different forms of wait statements. Explain with examples. (5)
(c) Write a test bench for the 4 bit comparator shown below. (5)



OR

- 14.(a) Briefly describe the two types of subprograms in VHDL. Write a function to convert a `std_logic_vector` to an integer. (10)
(b) Write the testbench for a 4 bit full adder. (5)
(c) Explain the transport and inertial delay in VHDL with the help of an example.(5)

MODULE III

- 15.(a) Write a behavioural VHDL model of a negative edge triggered D flip-flop using synchronous and active low preset and clear pins. Include tests for set up and hold time violation and assert if both preset and clear pins are given a 0. Assume Q and Qbar as the output. (8)
(b) Develop a VHDL code for a 4 bit (nibble) adder using structural description. (8)
(c) Implement a 2:4 decoder using selected signal assignment concurrent statements in VHDL. (4)

OR

- 16.(a) Write a VHDL model of an N bit counter with a control input. When the control input is '1', the counter counts up; and when it is '0' it counts down. When all the 1's and 0's are reached, the counter should stop. (8)
(b) Write a VHDL model for a priority encoder. (4)

(c) Write a VHDL description for a 8 bit Universal shift register with 'mode select' as the control pin. Depending upon the mode select, the actions given in the table has to be performed. (8)

Mode Select	Action
00	Hold
01	Shift right
10	Shift left
11	Parallel load

MODULE IV

- 17.(a) Explain, with example, what is meant by constraint in RTL synthesis. (5)
(b) Discuss the various steps involved in designing a digital system using FPGA. (10)
(c) List the features of Altera Flex 10K series CPLD's. (5)

OR

- 18.(a) Describe the architecture of CPLD with necessary diagrams. (10)
(b) List the features of Xilinx 4000 series FPGA's. (5)
(c) Explain the terms scheduling and binding in the context of behavioural synthesis. (5)