Question paper setters are requested to note the following instructions

1) Follow the text book , 6th edition of *Computer Organization and Embedded Systems* by Hamacher and Digital Logic and Computer Design by Morris Mano.
2) Instruction set of RISC machines may be asked (No programming) in general.

Fourth Semester B.Tech. Degree Examination (2013 Scheme)

Computer Science and Engineering

13.402 COMPUTER ORGANIZATION AND DESIGN (FR)

Model Question Paper

Time 3 Hours
Max. Marks 100

PART A

(*Answer **all** questions, each question carries **4** marks*)

1. (a) Write functions of the following registers (i) Program Counter (ii) Stack Pointer (iii) Instruction Register (iv) Link register

   (b) Register R4 and R5 of a processor contain the decimal numbers 2000 and 3000 before each of the following addressing modes are used to access a memory operand. What is the effective address in each case ? (i) 12 (R4) (ii) (R4, R5) (iii) (R4) (iv) 28(R4, R5)

2. Explain how nested subroutines is handled by the processor

3. Write the sequence of actions needed to fetch and execute the instruction ***Load R5, X(R7).***

4. (a) What is the difference between hard-wired control and microprogram control ? What are the advantages and disadvantages in each method ?
   (b) Two control functions at time T_2 are given as :
   Q_1T_2 : $A \leftarrow A + B, E \leftarrow C_{out}$
   T_2 : $P \leftarrow P - 1$
   What are the conditions to execute the above statements ?

5. A computer system uses 32- bit memory addresses and it has a main memory consisting of 1 G bytes. It has a 4 K-byte cache organized in the *block-set-associative* manner, with 4 blocks per set and 64 –bytes per block. Calculate the number of bits in each of the Tag, Set, and Word fields of the memory address.

PART B

(Answer **one full** question from **each module**, each full question carries **20** marks)

Module – I

6. (a) Discuss different addressing modes (with examples) used in RISC processors
   (b) What are vectored interrupts ? Write the sequence of actions carried out in response to an interrupt.
   (c) Draw a schematic diagram of interface used for keyboard and display. Explain functions of various registers in the interface. What are the different methods used for I/O transfer ?
7. (a)) Suppose that execution time for a program is proportional to instruction fetch time. Assume that fetching an instruction from the cache takes 1 time unit, but fetching it from memory takes 10 time units. Also, assume that a requested instruction is found in the cache with the probability 0.96. Finally, assume that if an instruction is

not found in the cache it must be first fetched from the main memory into the cache and then fetched from the cache to be executed. Compute the speed up ratio. What is the speed up ratio if the size of the cache is doubled and assuming that the probability of not finding a requested instruction is cut in half ?

(b) Write functions of condition code flags used in RISC processors. With an example, illustrate the need of overflow flag in addition to carry flag.

(c) Discuss different types instructions used in RISC processors

Module – II

8. (a) Draw the data path of five stage organization with multiplexers and inter-stage registers. Explain each stage of this organization.

   (b) At the time the instruction Load R6, 1000(R9) is fetched, R6 and R9 contain the values 4200 and 85320, respectively. Memory location 86320 contains 75900. Show the contents of the inter-stage registers RA, RB, RZ, RM and RY, where RA and RB are input to ALU and RZ stores output from ALU. RM is used to hold data to be stored in memory, and RY is an interstage register between RZ and register file.

9. (a) Design an adder / subtractor circuit with one selection variable s and two inputs A and B. When s = 0 the circuit performs A + B. When s = 1 the circuit performs A – B by taking the 2's complement of B.

   (b) Consider two ***n-*** bit binary numbers A and B, applied to the input of a parallel adder with all the n bits of B are 1s and C_{in} (carry in) is equal to zero. Show that the operation performed is then decrementing A.

Module – III

10. Explain with a figure, each functional unit of a Microprogram sequencer.

11. (a) Explain an organization of hardwired control unit CPU .

    (b) Distinguish between horizontal and vertical microinstructions. Discuss advantages and disadvantage of each scheme

Module – IV

12. a) Illustrate the implementation of an output interface for a display device. Explain function of each signal handled by the interface.

    b) Draw the timing diagram for Read operation on the PCI

13. (a) Explain the concept of Direct Memory Access (DMA)

    (b) Describe the organization of a 2M X 32 memory module using 512K x 8 static memory chip