SIXTH SEMESTER B.TECH DEGREE EXAMINATION
(2013 SCHEME)
Branch : Electronics and Communication Engineering
13.602: VLSI DESIGN (T)

Time: 3 Hours Max. Marks : 100

PART – A

(Answer all questions. Each question carries 2 marks.)

1. Why is the oxidation rate greater for the wet reaction in thermal oxidation?
2. State the laws governing the diffusion process?
3. What is meant by channeling? What is its effect in the doping profile for ion implantation?
4. Explain the effect of channel length modulation in the drain characteristics of MOSFET.
5. What is meant by switching threshold of a CMOS inverter? How is it related to the device size of PMOS and NMOS transistor?
6. Explain the layout design rules in VLSI.
7. Mention the causes for dynamic power dissipation in CMOS inverters.
8. Mention how the charge leakage problem can be reduced in dynamic logic design.
9. Explain how the 'write' operation is performed in 1T DRAM cell.
10. Implement a 4x4 NAND based ROM array using MOS ROM cell.

PART B

(Answer any one question from each Module.)

Module – I

11. (a) Explain the kinetics of thermal oxidation using Deal and Grove model. Clearly explain the terms 'linear rate 'and 'parabolic rate' constants related to this. (10)

(b) With neat diagrams, explain the steps involved in the fabrication of CMOS using n-well technology (* Show the top view / cross sectional view of the mask) (10)

OR

12. (a) Explain the steps involved in optical photolithography with the help of neat diagrams (5)
(b) Explain the CZ technique for crystal growth. Mention the advantage of float zone over CZ process. (5)
(c) What is meant by latch up in CMOS? Mention ways to minimize latch up. ((6)
(d) Explain the boundary layer problem in epitaxial process. Mention ways to minimize its effect in CVD. (4)

Module – II

13. (a) What is meant by 'scaling' in MOSFET? Explain the three different types of scaling. Clearly mention the advantages and disadvantages associated with each type of scaling. (10)
(b) What are the physical parameters affecting the threshold voltage of a MOSFET. In this context explain the substrate bias effect. (5)
(c) Explain 'hot electron effect' in short channel MOSFETs. How can it be minimized? (5)

OR

14. (a) Explain the different capacitances associated with MOS device and sketch the C-V characteristics for the MOSFET. (10)
(b) Explain the steps in VLSI design flow with the help of a suitable example. ((10)

Module – III

15. (a) Sketch the voltage transfer characteristics of a CMOS inverter and explain. (10)
(b) Derive the expression for short circuit power dissipation in a CMOS inverter. (6)
(c) Implement the function F=AB+A'C' +AB'C using transmission gate logic. ((4)

OR

16. (a) Show that in a CMOS inverter $V_{IL}=(3V_{dd}+2V_t)/8$ and $V_{IH}=(5V_{dd}-2V_t)/8$. Also find the noise margins. (Neglect velocity saturation and channel length modulation and assume $\beta n= \beta p$ and $Vtn= -Vtp$) (10)
(b) Implement a 16 bit carry select adder using 4 bit carry select adder blocks. (6)
(c) What are the features of dynamic logic? Explain charge sharing in dynamic logic. (4)

Module – IV

17. (a) What is the purpose of sense amplifiers? Explain the working of a differential sense amplifier (10)

(b) Explain scan based testing . (10)

OR

18. (a) Compare dynamic RAM and static RAM . Explain the ‘read’ and ‘write’ operations of a 6T SRAM cell with the help of neat diagrams. (10)

(b) Explain the general practices and concepts in CMOS testing. (10)