VI Semester B.Tech Degree Examination - 2012
Model Question Paper
13.602 VLSI DESIGN

Time:3 hrs max.marks : 100

PART-A

Answer ***all*** questions. Each question carries **2** marks

1. Differentiate between positive and negative photoresists.
2. State Fick's law of diffusion.
3. A proximity printer operates with a 20μm mask to wafer gap and a wavelength of 250nm. Find the minimum linewidth that can be obtained.
4. Define threshold voltage. Write the expression for threshold voltage under body bias condition.
5. Explain channel length modulation. How is it incorporated in the current relationship of MOS transistor?
6. Explain the junction capacitances associated with a MOSFET.
7. Illustrate a case of progressive transistor sizing to reduce propagation delay in CMOS design.
8. Pseudo NMOS is a ratioed logic. Justify.
9. How the test patterns are minimized by modeling the circuit with independent logic paths.
10. Consider a DRAM cell with Cs=50fF and Cbit=8Cs. Assuming a maximum voltage of Vs=Vmax=2.5V on the storage capacitor, what is the final voltage during a logic 1 read operation. (2x10 = 20 marks)

PART B

Answer one full question from each module

MODULE I

11. a) Portray the different steps involved in an n well process for CMOS. (12)
    b) With neat sketches, explain Czochralsky method of wafer processing. List the advantages and disadvantages of the process. (8)

OR

12. a) Derive Deal Grove model of oxidation. (10)
    b) With the aid of neat diagram explain ion implantation process (10)

MODULE II

13. a)Derive the current relationship in a MOS transistor in deep triode and saturation regions. (12)
    b) Define flatband voltage. Obtain an expression for threshold voltage of a MOS transistor in terms of flat band voltage and body effect parameter. (8)

OR

14. Elucidate the short channel effects in MOS with neat diagrams. (20)

MODULE III

15. Derive expressions for noise margin (NM_L and NM_H) and switching threshold of a CMOS inverter. (20)

OR

16. a) Design a 14 bit square root carry select adder. Calculate the worst case delay. (10)
    b) Explain the function of a 4 bit multiplier with block diagram. Write down the expression for maximum delay. (10)

MODULE IV

17. a) Draw the CMOS implementation of a NOR ROM cell to store 4 words of 4bits which are as follows 1011, 1110, 1101 and 1001. (10)
    b) Design a regular PLA structure using MOS to implement the function $Y_1= X_4$, $Y_2=X_1X_3+X_2 X_4$ and $Y_3=X_1X_2+X_2X_3$ (10)

OR

18. a) Explain the working of a 1 transistor DRAM cell with the help of timing diagrams.(10)
    b) Explain the methods of design for testability (10)